CSP ASSEMBLY RELIABILITY: COMMERCIAL AND HARSH ENVIRONMENTS

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ABSTRACT

The JPL-led CSP Consortium of enterprises representing government agencies and private companies has jointed together to pool in-kind resources for developing the quality and reliability of chip scale packages (CSPs) for a variety of projects. Last year (1), team members reported their experience on technology implementation challenges, including design and build of both standard and microvia boards, assembly of two types of test vehicles, and preliminary aging and thermal cycling test results on trial test vehicles. Since then, more than 150 test vehicles, single- and double-sided, have been assembled and are presently being subjected to various environmental tests. This paper presents the experience of three consortium team companies on characterizing reliability behavior under four different thermal cycling environments. Lessons learned on assembly are given in a paper included in this proceedings.

CSP IMPLEMENTATION CHALLENGES

Emerging grid chip scale packages (CSPs), and miniature versions of ball grid arrays (BGAs) are competing with bare die flip chip assemblies.

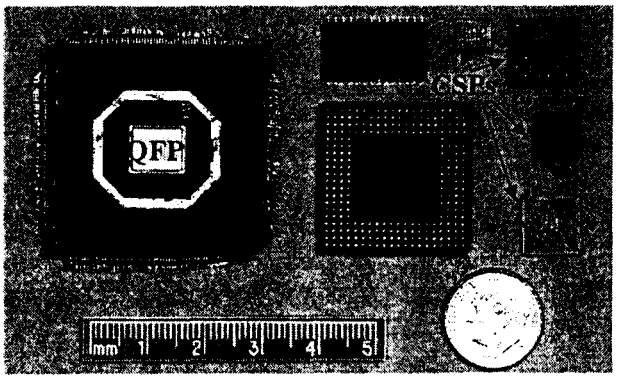

Figure 1 Miniaturization trend from QFP to BGA and CSP

Figure 1 shows the miniaturization trend from quad flat packages (QFP) to BGA and CSP. CSP is an important miniature electronic package technology for utilizing especially low pin counts, without the attendant handling and processing problems of low peripheral leaded packages such as thin small outline packages (TSOPs) and high I/O (input/output) QFPs. Advantages include self-alignment characterization during the assembly reflow process and better lead (ball) rigidity.

Figure 2 compares the advantages and disadvantages of CSP to bare die assembly.

Reliability data and inspection techniques are needed for CSP acceptance, especially for high reliability applications.

Chip Scale Package

Pros	Cons
• Near chip size	• Limited package/assembly data availability
• Testability for KGD (Known Good Die)	• Moisture sensitivity
• Ease of package handling	• Thermal management
• Robust assembly process	o High I/Os
o (Grid array version)	• Electrical performance
• Die shrink or expand	• Standards
• Standards	• Routability
• Infrastructure	o Microvia PWB for high I/Os
• Rework	• Underfill?
	• Reliability?
	• Infrastructure?

Figure 2 CSP advantages and disadvantages

In the process of building the NASA-JPL-industry CSP Consortium test vehicles, TVs, many challenges were identified regarding various aspects of technology implementation. Key challenges are summarized as follows.

Industry and "Expert" Definition of CSP

Although the expression "CSP" is widely used by industry both suppliers and users, its definition had evolved as the technology has matured. At the start of the package's introduction into the market, a very precise definition was adopted by a group of industry

experts. CSP was defined as a package that is up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Soon, it became apparent that suppliers were using the term CSP to promote a miniature version of a previous package.

A rapid transition to a much lower size was difficult both for package suppliers and end users. Suppliers had difficulty in building such packages whereas the users had difficulties in accommodating the need for the new microvia printed circuit board (PWB), chiefly, because of routing requirements and its increased cost. Other issues for accepting the "interim definition" by industry included needed maturity in assembly and infrastructure. For example, the use of pitches other than 0.5 mm, including 0.75 and 0.65, was aimed at using a standard PWB design rather than a microvia build to avoid the elevated cost of the latter.

The "expert definition" undermines one of the key purpose of the packages allowing for die shrinkage. If die shrinkage is acceptable for the package to retain the footprint, then a decrease in die size for the same CSP will change the term CSP for that package.

Therefore, in reality, CSPs are miniature new packages that industry is starting to implement, and there are many unresolved technical issues associated with their implementation. Technical issues themselves also change as packages mature. For example, in early 1997, packages with 1 mm pitch and lower were the dominant CSPs, whereas in early 1998 packages with 0.8 mm and lower became the norm for CSPs. New issues included the use of flip chip die rather than wire bond die in the CSP. Flip chip failure within the package is a potential new failure mechanism that needs to be considered.

Package Availability in Early 1997

CSP availability in daisy chain for the attachment reliability characterization was one of the challenging issues at the start of the program in early 1997. There were numerous publications on a wide range of CSPs, but most packages were in an early development stage and lacked package reliability information. Assembly reliability data were even rarer. Most packages were only available in prototype form, and this, of course, did not guarantee any similarity to the production version, or even the future availability of the package.

More than a six month delay in package delivery date was the norm. Four packages were not delivered at all, and one was delayed almost a year with a last moment modification by the supplier. Although many suppliers promoted their packages and package reliability, they were not willing to submit their packages for an independent evaluation, possibly because of lack of confidence.

At the start of the program, I/Os ranged from 12 to 540 to meet the short and longer term applications. The 540 I/O/ 0.5 mm package was dropped by the manufacturer prior to the trial test vehicle assembly. Three other higher I/O with 0.5 mm pitch were not delivered. For example, a hard metric, 0.5 mm CSP package with 188 I/Os having reliability data given by the supplier for its English pitch version was among these three packages. The supplier was unable to meet our last build scheduled in late 1998.

Lack of delivery clearly indicate that the package suppliers were struggling to build CSPs with 0.5 mm pitch, especially with high I/O counts. Therefore, by default, the maximum I/O package became a CSP with 275 I/Os.

The majority of the CSPs of the next phase of the CSP program have pitches of 0.8 mm. In this phase, there are a few high I/O CSPs with 0.5 mm pitch. This indicates that industry is starting to be more comfortable with moving towards a tighter pitch at higher I/O.

Issues

As discussed above, at the start of the program, CSPs were in their infancy. In addition to the difficulty of package availability at the time of assembly, there were other issues that needed to be resolved or tested.

For example, there were no guidelines or standard specifications for packages; therefore, in many instances package information was incomplete. Sometimes the package pitch was given in hard metric units and sometimes in English units (mil or inches). This led to dimensional errors because of decimal round off. There was no information on pad design relative to the package pad for achieving optimum reliability.

For example, the standards on various elements of CSPs were not available. The majority of packages were hard metric, however, a few with the inch pitches caused dimensional errors because of decimal round off when converted from inch to metric. There was no information on pad design relative to package pad for achieving optimum reliability.

For daisy-chain packages, it is possible to use a standard PWB design for low to high I/O packages. However for the active die, build up (microvia) board technology is required. Both standard and microvia technology were evaluated.

There were a number of packages from low I/O (<50) to higher I/O (about 300) for characterization. At the start of the program in early 1997, it became apparent that for the near future, 1-3 years, the dominant packages would be those with less than 50 I/Os. Specific application requirements could utilize packages with much higher I/Os.

A mixture of conventional SM (surface mount) packages, BGAs, flip chip, and CSPs with low to very high I/Os (about 500) on one board is another design and assembly challenge. Such a mixed technology board was designed, and its implementation issues are being studied by the JPL CSP consortium.

CSP TEST VEHICLE DESIGN

The Consortium agreed to concentrate on the following aspects of CSP technology after numerous workshops, meetings, and weekly teleconferences.

Package — Ten packages from 28 to 275 I/Os as listed in Table 1. The TSOP was used as control. Pitches varied from 0.8 mm to 0.5 mm, and 0.020 inches.

Printed Wiring Board (PWB) Materials and Build — The majority of boards were FR-4. A few boards were made of BT (bismaleimide triazine) and also high temperature epoxy were included for evaluation. The PWBs were double sided, standard and microvia. In designing daisy chains, it became apparent that the standard PWB technology could not be used for routing the majority of packages.

Table 1 CSP Package Configurations Matrix

Package ID	Package Type	Package Size (mm)	Pad Size (mm)	Pitch (mm)	I/O Count	Package. Thickness (mm)	Ball Dia. (mm)
A	Low I/O Wafer	1.6 x 3.2	0.25 x 0.15	0.5	12	0.5	0.075
B	Leadless-1	7 x 13.6	0.35 x 0.7	0.8	28	0.8	-
C	TAB CSP-2	7.43 x 5.80	0.4	0.75	40	0.885	0.3
D	TSOP44	18.61 x 10.36	0.27 x 0.5	0.8	44	1.13	n/a
E	Leadless-2	7 x 12.3	0.30 x 0.75	0.5	46	0.8	n/a
F	TAB CSP-1	7.87 x 5.76	0.4	0.75	46	0.91	0.3
G	Chip on Flex-1 (COF-1)	0.3" x 0.3"	.010 in.	.020 in.	99	1.75	0.3
H	CSP-Redistribution-1	10.025 x 8.995	0.254	0.5	96	-	0.3
I	CSP Redistribution-2	6.22 x 5.46	0.254	0.5	99	-	0.3
J	Wire Bond on Flex-1	12.1 x 12.1	0.375	0.8	144	1.4	0.5
K	Wire Bond on Flex-2	12 x 12	0.25	0.5	176	0.5	0.3
L	TAB CSP-3	13.1 x 13.1	0.3	0.5	188	0.5	0.3
M	Chip on Flex-2 (COF-2)	0.5 x 0.5	.010 in.	.020 in.	206	1.75	0.3
N	Ceramic CSP	15 x 15	0.4	0.8	265	0.8	0.5
O	Wafer Level	0.413 x 0.413	.010 in.	.020 in.	275	-	0.3

- All measurements are in mm unless otherwise specified
- Packages A, H, L, and L were not available at the time of assembly

Daisy-Chain — Packages had daisy chain patterns . In most cases, these patterns were irregular and much time and effort was required for design. This was especially cumbersome and difficult for packages with higher I/Os, and many daisy-chain mazes were developed on the PWB to complete the chain loop into the package through solder joint.

Surface finish — The majority of PWBs had organic solder preservative (OSP) surface finish. A limited number utilized other surface finishes, including hot air solder leveling (HASL), electroless Au/Ni, and immersion silver. Electrolytic Ni/Au surface finish did not prove successful. The majority of solder pastes used during assembly were no-clean which is becoming the

norm for commercial assemblies. Water soluble (WS) and rosin mildly activated (RMA) pastes were also included because of the specific needs of some of the team members, e.g., JPL.

Underfill — The majority of assemblies did not require underfill. A limited numbers were underfilled to understand if any improvement would be achieved. One package required underfilled because of its known low reliability without underfill.

Double-Sided Assembly — The PWBs were double-sided, and several boards with packages on both sides were assembled to investigate the reliability of single sided versus double-sided test vehicles, as well as standard versus microvia technology.

When packages were placed on both sides, the two sides were not mirror images. The packages were rotated a 90° angle relative to one another. The 90° rotation provided additional insight regarding the reliability to the effect of double-sided assemblies on reliability that realized at a later stage. The effect of mirror image double-sided assemblies, as well as various offsets, can be determined by this test vehicle.

Solder Volume — Three stencil thicknesses were included: high, standard, and low. The two extreme thicknesses were 4 (low) and 7 mil (high) with a different stencil aperture design depending on the pad size. The standard stencil thickness which was used for the majority of test vehicles, was 6 mil thickness.

Test Vehicle Feature — The test vehicle was 4.5 by 4.5 inches and divided into four independent regions. For the single-sided assembly, most packages can be cut for failure analysis without affecting the daisy-chains of the other packages. All packages were daisy-chained, and they had up to two internal chain patterns.

Environmental testing — To link the data to those generated for the Ball Grid Array Consortium test, two conditions of –30° to 100°C (cycle A) and –55° to 125°C (Cycle B) were included. Two additional cycles were also investigated. Thermal cycling in the range of 0° to 100°C was performed to meet the needs of the commercial team members.

Hence, four different thermal cycle profiles were used. These were:

- Cycle A: The cycle A condition ranged from –30° to 100°C and had an increase/decrease heating rate of 2° to 5°C/min and dwell of about 20 minutes at the high temperature to assure near complete creep of the solder. The duration of each cycle was 82 minutes.
- Cycle B: The cycle B condition ranged from –55° to 125°C, with a very high heating/cooling rate. This cycle represent near thermal shock since it utilized a three region chamber: hot, ambient, and cold. Heating and cooling rates were nonlinear and varied between 10 to 15 °C/min with dwells at the extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes.
- Cycle C: The cycle C condition ranged from –55° to 100°C with a short time duration at low temperature. The heating and cooling rates were 2° to 5°C/min with a dwell at maximum temperature of more than 10 minutes.. The duration of each cycle was 90 minutes.
- Cycle D: The cycle D condition ranged from 0° to 100 °C with a 2-5°C/min heating/cooling rate. The Dwell at the extreme temperatures was at least 10 minutes, the cycle duration was 73 minutes.

Monitoring — The test vehicles were monitored continuously during the thermal cycles for electrical interruptions and opens. The criteria for an open solder joint specified in IPC-SM-785, Sect. 6.0, were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, there were many additional interruptions within 10% of the cycle life.

ASSEMBLY

The Consortium assembled two different test vehicle types. Preliminary assembly results for the first type (TV1) and reliability test results for the trial test vehicles were presented elsewhere(1). For full production, about 150 test vehicles with the many variables discussed above were built. The photograph of an assembled test vehicle, with its packages, face up, is shown in Figure 4. A drawing for the Figure 4 double-sided test vehicle in which the back side package outlines are also apparent is shown in Figure 5. Note that a few packages were imaged to different packages with a 90° rotation in a double-sided test vehicle.

Wide Distribution of Daisy Chain Resistances

The daisy chain resistance of an assembled package depends on both package and board design parameters. Once these parameters are set, resistances should fall within a narrow range. A deviation from the norm value represents manufacturing defects.

Resistances for CSP assemblies were measured by a hand held multimeter. Several unrealistically large resistance values were observed for three packages. Initially, it was thought that defects due to the daisy chain design might be the source. Further investigation revealed that the package supplier source and package types were the cause of such variations.

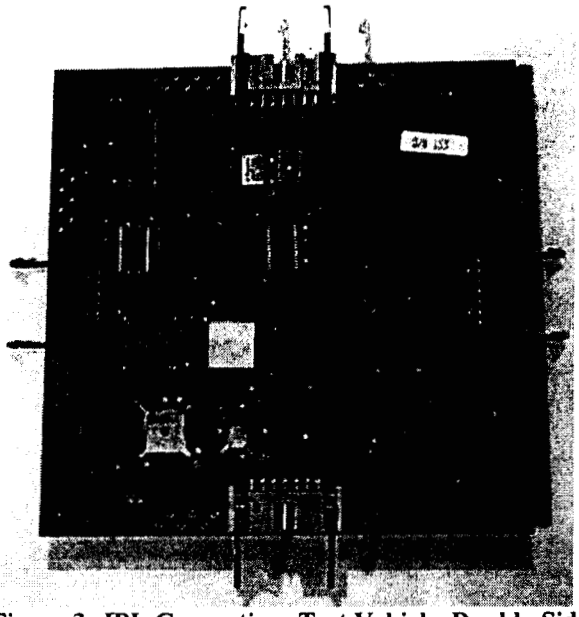

Figure 3 JPL Consortium Test Vehicle, Double-Sided

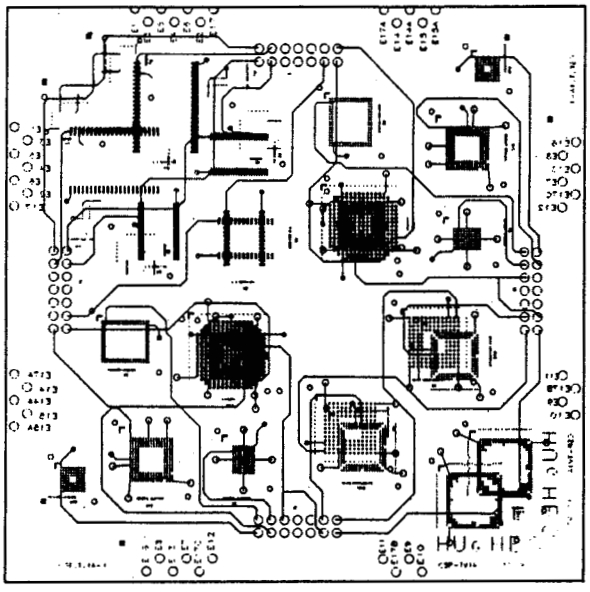

Figure 4 Double-Sided Test Vehicle and Regions of Package Overlaps

Figure 5 presents the cumulative distribution of resistance values for nine package assemblies. A small deviation from the norm values are acceptable since these were measured manually. The values depend on how long the meter is allowed to be stablized and what are the resistances for the two probes. A noticeable high resistance values represent most probably a manufacturing defect. These are shown by arrows towards the top end cumulative distributions in this Figure. Assemblies with such defects are expected to fail much earlier than their norm. In our case, several of manufacturing variables were intentionally introduce to determine the effects of such variables on reliability. Two of manufacturing variables were change of stencil thickness and placement offsets.

Effects of package lot source apparent from J144, wire-on-flex (WOF), plots of accumulative daisy-chain resistance. One sets had a resistance value of about 2 Ω and the other about 87 Ω, each with relatively a narrow distribution. The package lot was apparent from a marking on the package for each category; therefore, the possibility that such variations were due to board or assembly was rejected. Package K176, WOF, from the same vendor showed a more narrower resistance distribution. Resistance values were higher than J144, but their values were close to one of the lot source.

Resistance values for M206, chip-on-flex (COF), were unrealistically high, nearly 700 Ω. Resistance measurement of two adjacent balls within the package were high, narrowing the cause of high value to package. These results may indicate that the trace fabrication process for this technology is the source of high resistance. Further comparison of results for the JPL CSP consortium will further shed light on these issues.

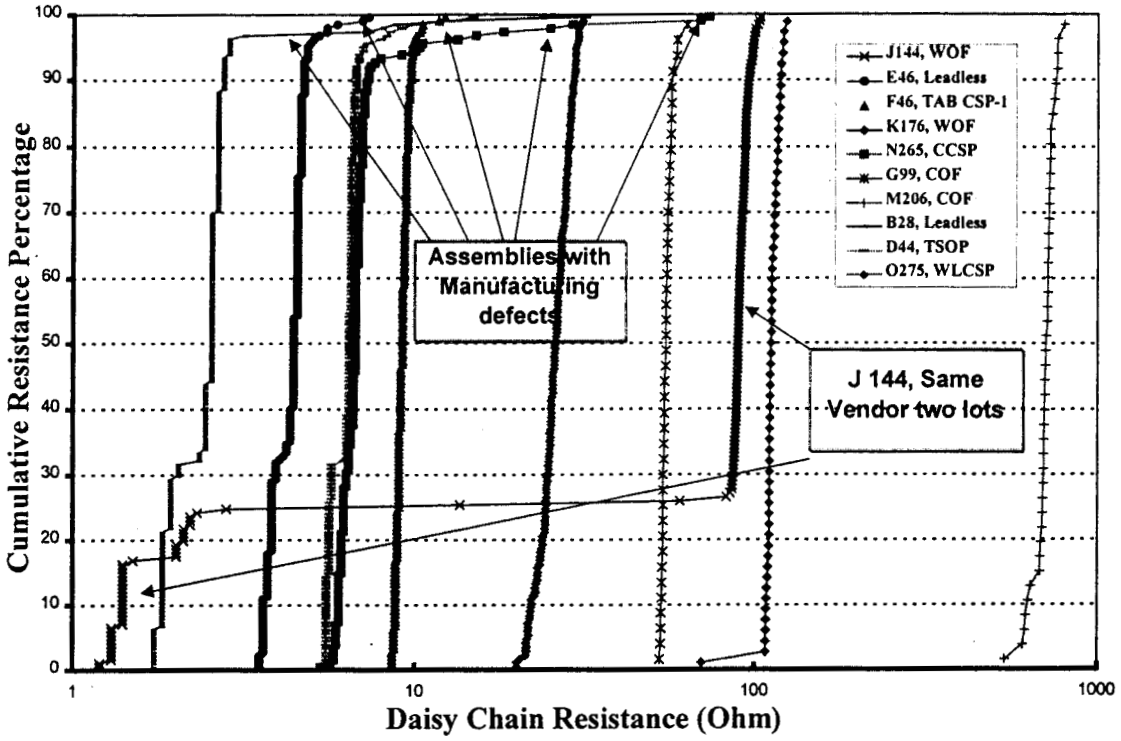

Figure 4 Cumulative Resistance for CSP Assemblies,

ENVIRONMENTAL TEST RESULTS

A large number of assemblies have already failed, and their cycles to failure have been documented. Out of these, cycles to failure data for three packages under four thermal cycling conditions are reviewed. Results for two chip on flex assemblies and leadless assemblies on single and double sided test vehicles are also presented.

Cycles to Failures for Chip on Flex Assemblies

Figure 5 shows cycles to failure for the two chip on flex packages with two different I/Os under the same thermal cycling conditions. Test results are for 99 I/O and 206 I/O packages subjected to cycle A condition (-30°/100°C). The cycles to failure distribution for the higher I/O assembly is much narrower than its lower I/O package. One may even note two possibly distinct failure distribution for the G99 I/O assemblies. The reason for the two failure trends are yet to be identified.

Figure 6 compares cycles to failure test results for the G package with 99 I/Os under four thermal cycling conditions. The trends are as expected, i.e., as the thermal cycling temperature ranges increase, the cycles-to-failure decrease. Note that assemblies failed between 3 to 34 cycles under a near thermal shock in the range of –55° to 125 °C (B condition). Cycles-to-failure was 152 cycles under a typical commercial thermal cycling conditions in the ranges of 0° to 100°C. Results for –55°/100°C and –30°/100°C were between the two extreme cycling conditions as expected.

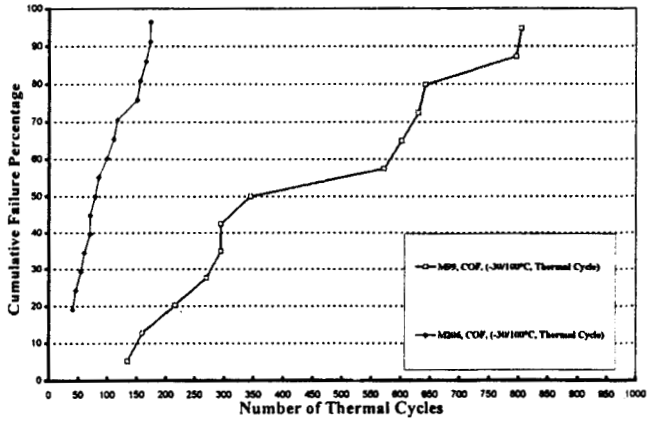

Figure 5 Cumulative Failure Distribution for Flex on Chip Assemblies with 99 and 206 I/Os

These data will be used to see the effects of both maximum and minimum temperature changes as well as how well they will follow projection models such as Coffin-Manson relationship.

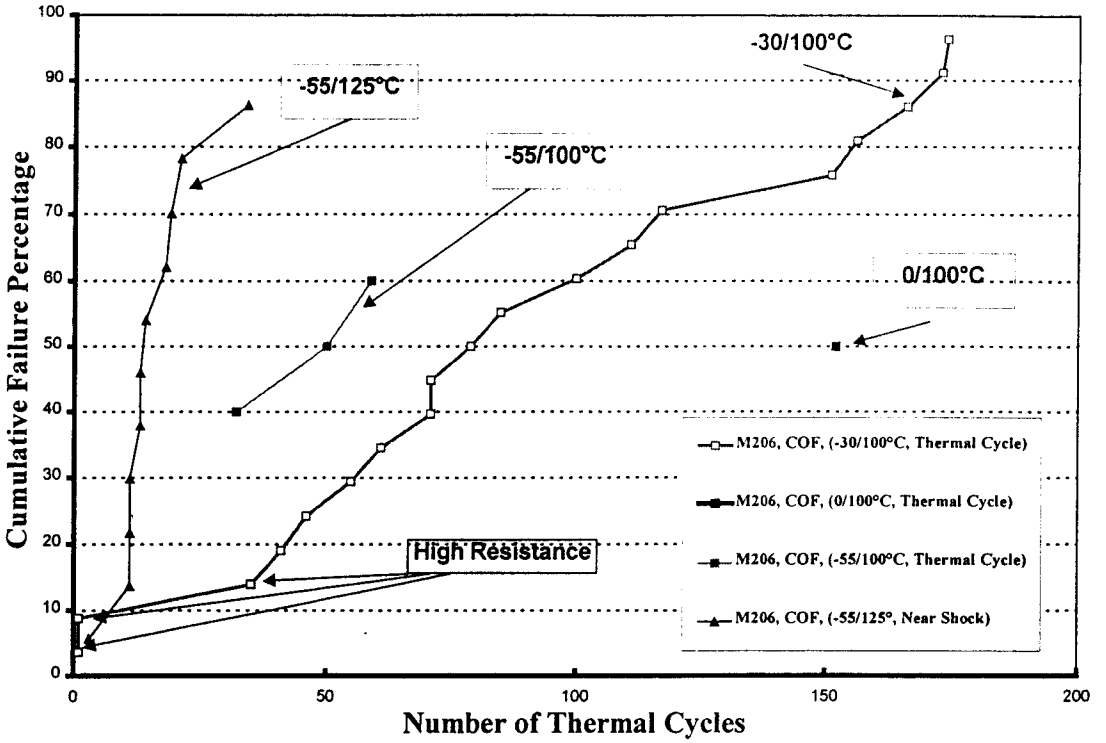

Figure 6 Cumulative Failure Distribution for Flex on Chip Assemblies with 206 I/Os Under Four Thermal Cycle Conditions

X-ray Inspection under exaggerated condition

One M206 assembly, which failed at 35 cycles in the range of –30°/100 °C, was inspected after it was further cycled to 500. By further cycling, we were able to exaggerate the cracking and separation of solder balls/joint. This allowed the clear observation of solder joint openings that are generally impossible to detect when they have just failed. Figure 7 shows an X-ray photomicrograph of an exaggerated failure. It is apparent that separation occurred either from the package site or board site

Single and Double-Sided Mirror-imaged

Figure 8 shows thermal cycling test results for package B, a leadless assembly with 28 I/Os, under two conditions for both single and double sided assemblies. The assembly location on the board was such that in a double sided assembly, it was a direct mirror image of itself with a 90° rotation (see Figure 4).

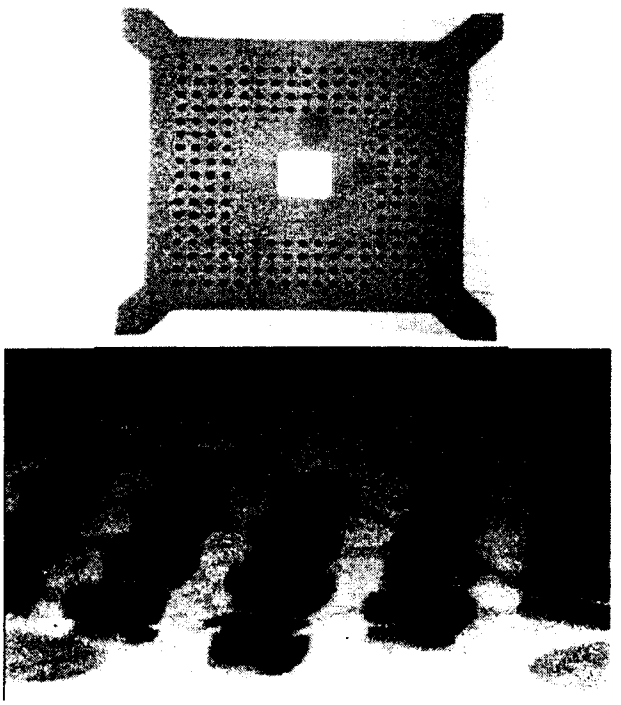

Figure 7 Exaggerated X-rays showing failure from either package or board sites

The single-sided assemblies failed at much higher cycles that double-sided assemblies. The N50 (cycles to 50% failure) were 437 for double- and 763 for single-sided assemblies under cycle A condition (-30°/100 °C). The double sided assemblies also failed much earlier than single sided assemblies under other thermal cycling conditions. As an example, results for double sided assemblies under –55°/125°C is also included in this Figure.

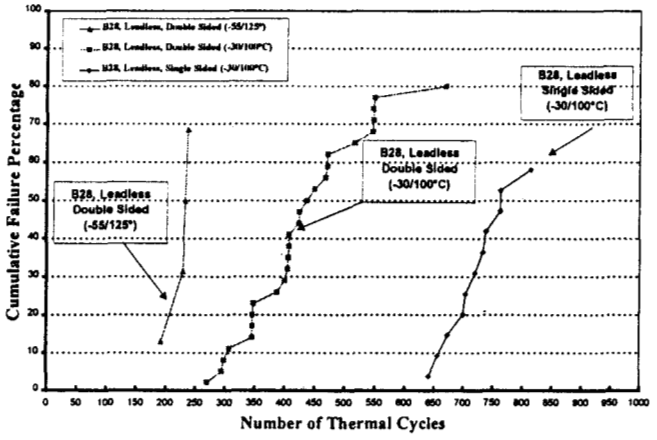

Figure 7 Single and Double Sided Assembly Failure Comparison

CONCLUSIONS TO DATE

- The Majority of CSPs with 0.5 mm pitch were not ready at the time of assembly in mid 1998. One possible reason could be a concern about their reliability by the manufacturer.

- Assembly daisy-chain values were from 2 Ω to 700 Ω and for a package from two different lots were significantly different. CSP package resistance was found to be the cause.

- One package required underfilling, and three others showed very low cycles to failures. Underfilling might be a requirement for these packages even for relatively benign commercial applications.

- Cycles-to-failure trends for one assembly under four different environments were different, and the trends were as expected. This means, as temperature cycling ranges increased, cycles-to-failure decreased.

- Single-sided assemblies showed about 40 percentage higher cycles-to-failure than double-sided mirror imaged leadless packages.

- Failures for one assembly were either from board or package. This is similar to BGA failure reported by the JPL BGA consortium (2).

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ACKNOWLEDGMENTS

The majority of research described in this publication is being conducted by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

I would like to acknowledge the in-kind contributions and cooperative efforts of the JPL MicrotypeBGA consortium. Special thanks to E. Siméus, S. Stegura, R. Smedley, Raytheon; A. Chen, I. Sterian, Celestica; R. Chanchani, Sandia; and other team members who have been contributors to the progress of this program.